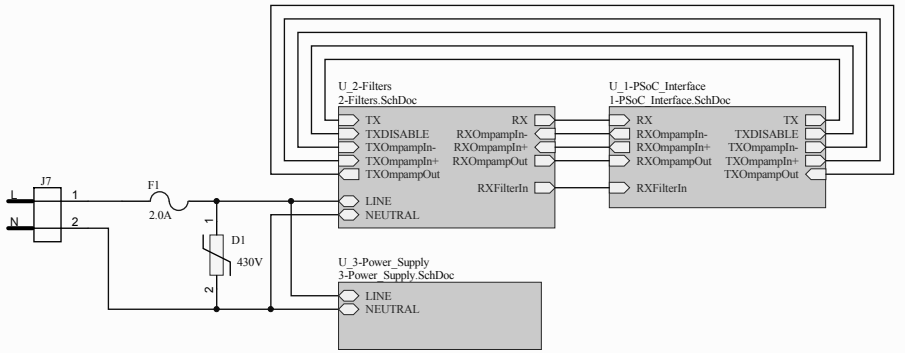


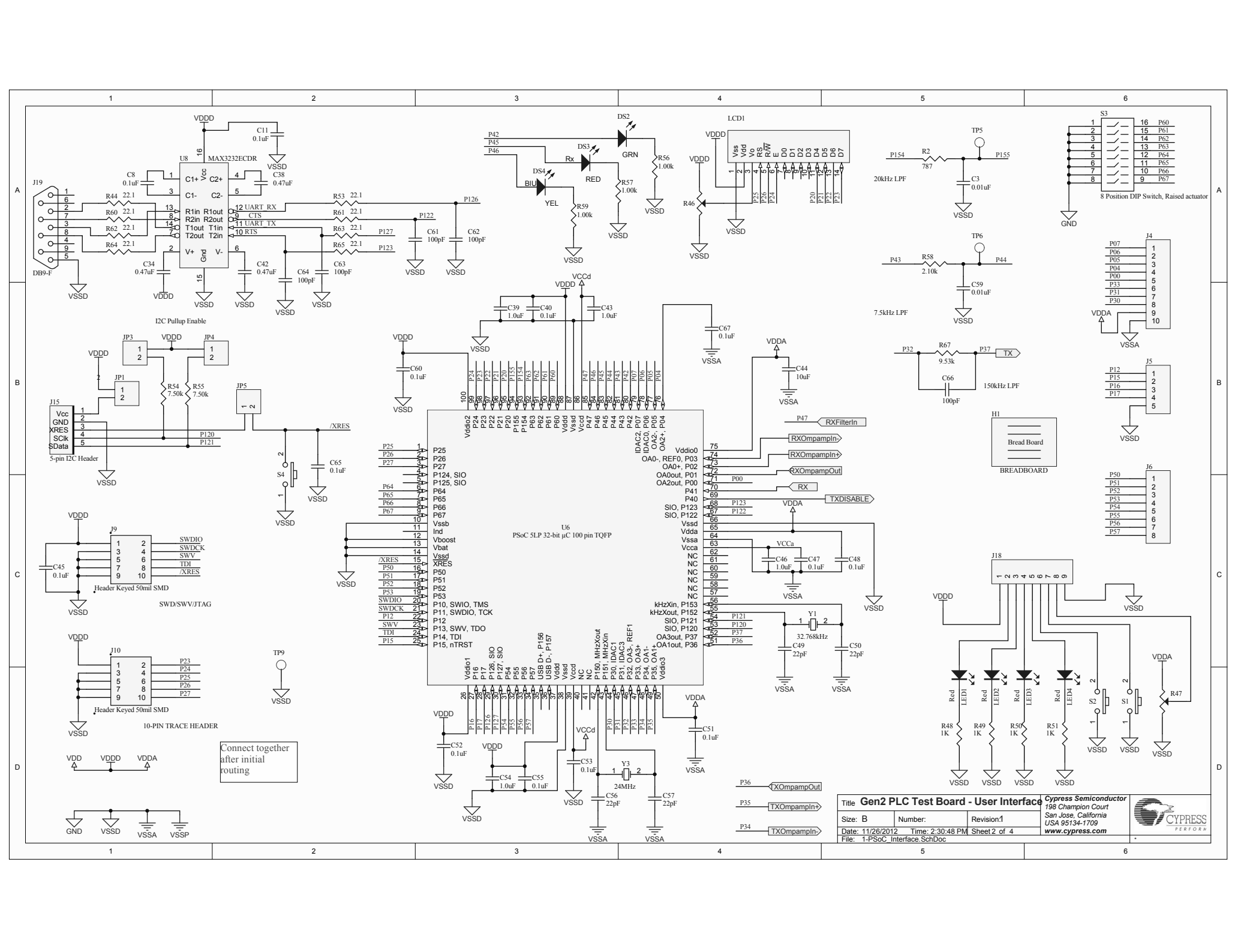
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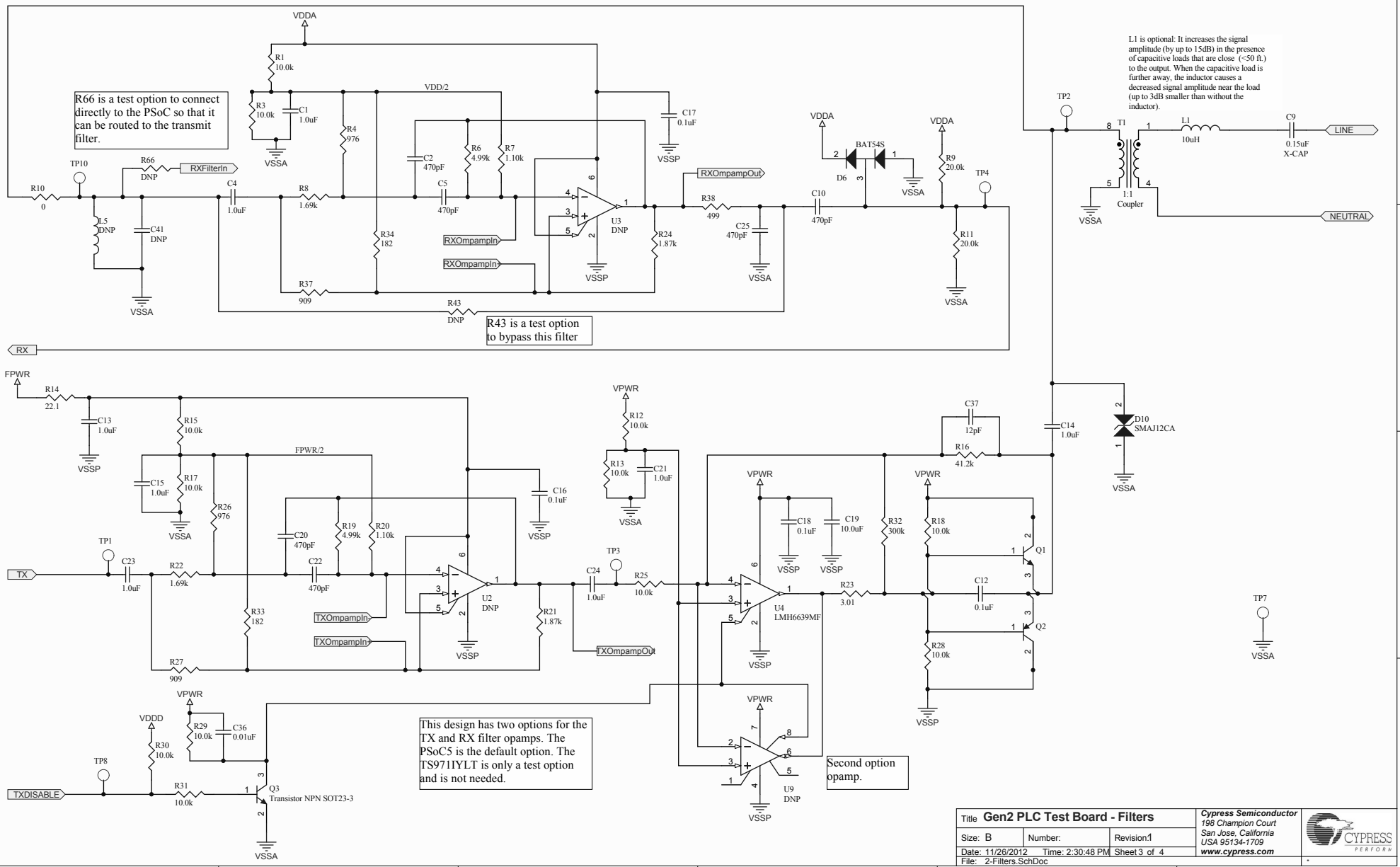
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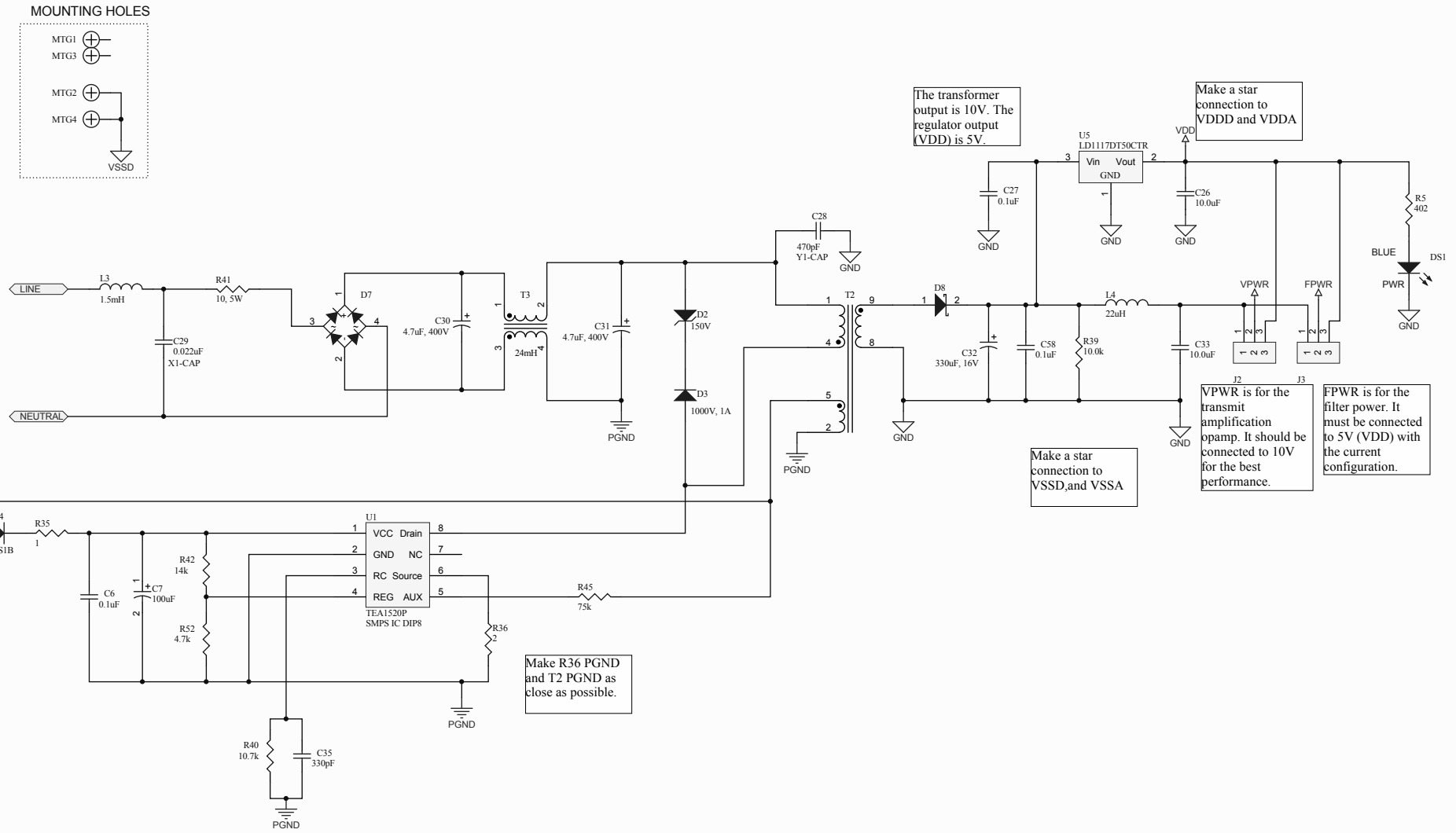
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Title **Gen2 PLC Test Board**			
Size: B	Number:	Revision1	
Date: 11/26/2012 Time: 2:30:47 PM	Sheet 1 of 4		
File: Top Level.SchDoc			

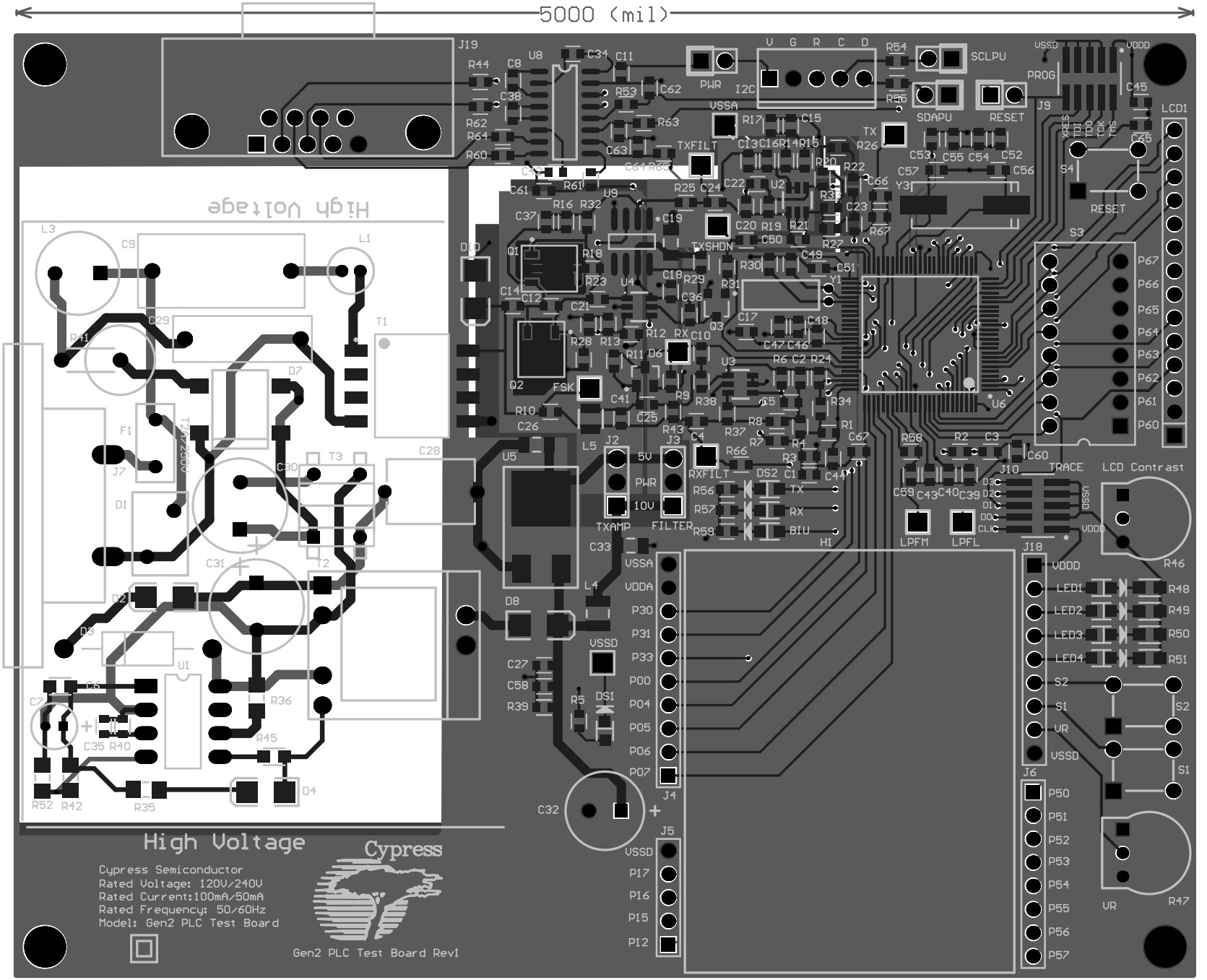
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U8
MAX3232ECDR
DB9-F
I2C Pullup Enable
5-pin I2C Header
SWD/SWV/JTAG
Header Keyed 50mil SMD
10-PIN TRACE HEADER
Connect together after initial routing
U6
PSoC 5LP 32-bit µC 100 pin TQFP
LCD1
DS2
GRN
DS3
RED
DS4
YEL
20kHz LPF
7.5kHz LPF
150kHz LPF
8 Position DIP Switch, Raised actuator
BREADBOARD
32.768kHz
24MHz
Title Gen2 PLC Test Board - User Interface
Size: B
Number:
Revision1
Date: 11/26/2012 Time: 2:30:48 PM Sheet 2 of 4
File: 1-PSoC_Interface.SchDoc
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R66 is a test option to connect directly to the PSoC so that it can be routed to the transmit filter.
L1 is optional: It increases the signal amplitude (by up to 15dB) in the presence of capacitive loads that are close (<50 ft.) to the output. When the capacitive load is further away, the inductor causes a decreased signal amplitude near the load (up to 3dB smaller than without the inductor).
R43 is a test option to bypass this filter
This design has two options for the TX and RX filter opamps. The PSoC5 is the default option. The TS9711YLT is only a test option and is not needed.
Second option opamp.
VDDA
VDD/2
VPWR
FPWR
FPWR/2
VDDD
VSSA
VSSP
RX
TX
TXDISABLE
RXFilterIn
RXOmpampIn
RXOmpampOut
TXOmpampIn
TXOmpampOut
LINE
NEUTRAL
U3 DNP
U2 DNP
U4 LMH6639MF
U9 DNP
Q3 Transistor NPN SOT23-3
BAT54S
1:1 Coupler
D10 SMAJ12CA
Title Gen2 PLC Test Board - Filters
Size: B
Number:
Revision1
Date: 11/26/2012 Time: 2:30:48 PM Sheet 3 of 4
File: 2-Filters.SchDoc
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Title **Gen2 PLC Test Board - Power**			**Cypress Semiconductor** 198 Champion Court San Jose, California USA 95134-1709 **www.cypress.com**
Size: B	Number:	Revision1	
Date: 11/26/2012 Time: 2:30:48 PM	Sheet 4 of 4		
File: 3-Power_Supply.SchDoc			



Top Layer
Ground Layer
Power Layer
Bottom Layer

Top Overlay
Bottom Overlay

Mechanical 1

Multi-Layer